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09/745,549	12/26/2000	David J. Sager	2207/5913	8722

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,549	SAGER ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,10-13,15-24,28-35 and 37-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,10-13,15-24,28-35 and 37-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 8, 10-13, 15-24, 28-35, and 37-42 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Extension of Time and Amendment as received on 8/23/2005.

Amendment Format Comments

3. In the future, please omit the statement "Please add the following new claims" (page 9 of the amendment). The claims are no longer new, and even if they were new, the "(New)" status identifier is sufficient enough to indicate new claims.

Drawings

4. The drawings are objected to because of the following minor informalities: It is asked that applicant increase the size of the reference numbers listed in Fig.1, Fig.2, and Fig.3, because they are very difficult to read. The numbers in Fig.4-5 are sufficient. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and

appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 8 is objected to because of the following informalities: In the 2nd to last line, replace "modified second register" with --modified second renamed register--.

6. Claim 10 is objected to because of the following informalities: In the 4th to last line, replace "second register" with --second renamed register--.

7. Claim 11 is objected to because of the following informalities:

- The preamble does not appear to be grammatically correct and it is not understood by the examiner.
- In line 2, remove the space between "instruction" and the comma.

8. Claim 19 is objected to because of the following informalities: In line 9, replace "said source register and destination register" with --said first and second source registers and said destination register".

9. Claim 28 is objected to because of the following informalities:

- In line 4, replace "same as on" with --same as one--.

- In the last two lines, replace "the destination register" with --the renamed destination register--.

10. Claim 29 is objected to because of the following informalities:

- In line 3, replace "register" with --registers--.
- In the last line, replace "source register" with --renamed source register--.

11. Claim 31 is objected to because of the following informalities:

- In line 5, replace "same as on" with --same as one--.
- In the last two lines, replace "the destination register" with --the renamed destination register--.

12. Claim 32 is objected to because of the following informalities: In line 9, replace "the result register" with --the renamed result register--.

13. Claim 34 is objected to because of the following informalities: In line 3, replace "register" with --registers--.

14. Claim 37 is objected to because of the following informalities: In the 2nd to last line, replace "first register" with --first renamed register--.

15. Claim 39 recites the limitation "the addition results" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 20-24 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

18. Claim 20 recites the limitation "the source register" in line 3. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 21 recites the limitation "the renamed source register" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 22 recites the limitation "the renamed source register" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 8, 10-13, 15-24, 28-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent No. 6,334,183 (as applied in the previous Office Action and herein referred to as Blomgren) in view of Yeager et al., U.S. Patent No. 5,758,112 (herein referred to as Yeager).

23. Referring to claims 11 and 34, Blomgren has taught a method of sub-register data operations in executing an instruction, the method comprising:

a) designating first and second operand registers and a result register, the result register being the same as one of the operand registers. See Fig.2 and note the ADD BH,AL->AL instruction, which has a first operand BH, a second operand AL, and a result register AL, which is the same as the second operand.

b) Blomgren has not taught renaming each of the registers as a register within a plurality of registers such that each of the registers is a different register. However, Yeager has taught the basic idea of register renaming. See Fig.2 and column 7, lines 35-43. Essentially each destination register is renamed to a register in the free list and each source register is renamed to the register that is has been previously mapped to. As is known in the art, register renaming allows for the elimination of WAR (write-after-read) and WAW (write-after-write) hazards. This, in turn, would increase throughput because hazards would be eliminated, and hazards are responsible for stalling the processor. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Blomgren to include register renaming.

c) Blomgren has further taught executing the instruction on a first renamed register and a second renamed register. See Fig.2, and note the ADD BH,AL->AL instruction, for instance. B and A would be first and second renamed registers.

d) Blomgren in view of Yeager has further taught preventing the propagation of a carryover of a result of the executed instruction from low-order bit positions of a renamed result register to high-order bit positions of the renamed result register. See Blomgren, Fig.2, and note that in the case of the ADD BH,AL->AL instruction, adder 164 will add two 8-bit numbers and produce an 8-bit result. Even if both numbers were 11111111, which when added would normally produce a carry, adder 164 does not produce or propagate a carry. See column 11, lines 25-29.

e) Blomgren in view of Yeager has further taught merging the result of the executed instruction with a plurality of high-order bits from the first renamed register, the plurality of high-order bits being copied into the high-order bit positions of the renamed result register, and the result being placed into low-order bit positions of the renamed result register. See Blomgren, Fig.2, and note that when the ADD BH,AL->AL instruction is executed, the result from adder 164 is placed in the lower 8 bits of the result and merged with high-order bits passed on from 168 and 170.

24. Referring to claims 8 and 35, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren has further taught that the merging a result comprises: modifying contents of the second renamed register by placing data values of zero in the high-order bit positions of the second register; adding contents of the first renamed register with the modified second register; and placing the result in the renamed result register. See Fig.2, and column 10, lines 31-41, and column 9, line 64, to column 10, line 10.

5. Referring to claims 10 and 37, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren has further taught that the merging a result comprising: modifying contents of the first renamed register by placing data values of zero in the low-order bit positions of the first renamed register; modifying contents of the second renamed register by placing data values of zero in the high-order bit positions of the second register; adding the modified first renamed register with the modified second renamed register; and placing the result in the renamed result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the instruction ADD BL,AH->AH the lower portion of B is added to the middle portion of A, which results in the counterparts being zeroed).

6. Referring to claim 12, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren has further taught that the first renamed register and the second renamed register have 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

7. Referring to claim 13, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren has further taught that the renamed result register has 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

8. Referring to claim 15, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren has further taught that the result of the executed instruction is less than 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the result is an 8-bit result in the case of the ADD BH,AL->AL instruction).

9. Referring to claim 16, Blomgren in view of Yeager has taught a method as described in claim 15. Blomgren has further taught that the result of the executed instruction is less than or equal to 16 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the result is an 8-bit result in the case of the ADD BH,AL->AL instruction).

10. Referring to claim 17, Blomgren in view of Yeager has taught a method as described in claim 16. Blomgren has further taught that the result of the executed instruction is less than or equal to 8 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the result is an 8-bit result in the case of the ADD BH,AL->AL instruction).

11. Referring to claim 18, Blomgren in view of Yeager has taught a method as described in claim 16. Blomgren has further taught that the merging a result is performed before instruction execution is complete (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; the

result and the unchanged portion of the register are available to the destination register at the same time).

12. Referring to claim 19, Blomgren has taught a processor comprising:

a) an instruction set having an instruction. See Fig.2.

b) first and second source registers and a destination register referenced by the instruction from the instruction set, one of said source registers and said destination register being the same. See Fig.2 and note the ADD BH,AL->AL instruction, which has a first operand BH, a second operand AL, and a result register AL, which is the same as the second operand.

c) Blomgren has not taught a register renamer including a plurality of registers and a lookup table linking first and second renamed source registers and a renamed destination register in said plurality of registers to said source register and destination register, the renamed destination register being different than either of said first and second renamed source registers. However, Yeager has taught such a concept. See Fig.2 and column 7, lines 35-43. Essentially each destination register is renamed to a register in the free list (a new, different register) and each source register is renamed to the register that is has been previously mapped to. As is known in the art, register renaming allows for the elimination of WAR (write-after-read) and WAW (write-after-write) hazards. This, in turn, would increase throughput because hazards would be eliminated, and hazards are responsible for stalling the processor. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Blomgren to include register renaming.

d) Blomgren in view of Yeager has further taught a logic circuit to examine the instruction before execution to identify a portion of one of said renamed source registers that should remain

unchanged into the renamed destination register, and the logic circuit further to move the unchanged portion from one of the renamed source registers into the renamed destination register before instruction execution is complete. See Blomgren, abstract, Fig.2, and column 9, line 64, to column 10, line 10; as shown in Fig.2, when the ADD BH,AL->AL instruction is executed, the unchanged portion of the register is passed though while the result of the lower portion of the registers is calculated.

e) the logic circuit including a carryover circuit to prevent propagation of a carryover from the execution of the instruction to the unchanged portion of the renamed destination register. See Blomgren, Fig.2, and note that in the case of the ADD BH,AL->AL instruction, adder 164 will add two 8-bit numbers and produce an 8-bit result. Even if both numbers were 11111111, which when added would normally produce a carry, adder 164 does not produce or propagate a carry. See column 11, lines 25-29.

13. Referring to claim 20, Blomgren in view of Yeager has taught a processor as described in claim 19. Blomgren has further taught that the logic circuit is to move the unchanged portion into the renamed destination register by setting corresponding values of the source register to zero. See the abstract, figure 2, column 9, line 64, to column 10, line 41).

14. Referring to claim 21, Blomgren in view of Yeager has taught a processor as described in claim 19. Blomgren has further taught that the renamed source register and the renamed destination register have a greater bit-length than a result of the instruction (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the registers are 32 bits wide and the result is an 8-bit result that is written to bits 0:7 of the destination register).

15. Referring to claim 22, Blomgren in view of Yeager has taught a processor as described in claim 21. Blomgren has further taught that the renamed source register and the renamed destination register each has 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

16. Referring to claim 23, Blomgren in view of Yeager has taught a processor as described in claim 21. Blomgren has further taught that the result of the instruction has less than 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the result is an 8-bit result that is written to bits 0:7 of the destination register).

17. Referring to claim 24, Blomgren in view of Yeager has taught a processor as described in claim 23. Blomgren has further taught that the result of the instruction is less than or equal to 16 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; note that the result is an 8-bit result that is written to bits 0:7 of the destination register).

18. Referring to claims 28 and 31, Blomgren has taught a method comprising:

a) receiving an instruction to perform an operation on contents of first and second source registers and store the results of the operation in a destination register, the destination register being the same as one of the source registers, the contents including a plurality of bits and the operation results being a different bit length then bit lengths of the first and second source registers. See Fig.2 and note the ADD BH,AL->AL instruction, which has a first operand BH, a second operand AL, and a result register AL, which is the same as the second operand. Also, as shown in Fig.2, and in the specification, the result of 8 bits from adder 164 is smaller than the 32 bit registers).

b) Blomgren has not taught renaming the first and second source registers and the destination register as first and second renamed source registers and a renamed destination register, from among a plurality of registers, the renamed destination register being different than either the first or second renamed register. However, Yeager has taught such a concept. See Fig.2 and column 7, lines 35-43. Essentially each destination register is renamed to a register in the free list (a new, different register) and each source register is renamed to the register that is has been previously mapped to. As is known in the art, register renaming allows for the elimination of WAR (write-after-read) and WAW (write-after-write) hazards. This, in turn, would increase throughput because hazards would be eliminated, and hazards are responsible for stalling the processor. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Blomgren to include register renaming.

c) Blomgren in view of Yeager has further taught identifying high order bits of one of the renamed source registers that are to remain unchanged when merged into the renamed destination register. See Blomgren, Fig.2, and note that for the ADD BH,AL->AL instruction, components 170 and 168 just pass bits on unchanged to be merged.

d) Blomgren in view of Yeager has further taught modifying the contents of the other renamed source register by setting corresponding high order bits of the other renamed source register to zero. See Blomgren, column 10, lines 31-41, and note that the corresponding bits of the second operand are zeroed.

e) Blomgren in view of Yeager has further taught adding the contents of the one of the renamed source registers with the modified contents of the other renamed source register. See Fig.2.

f) Blomgren in view of Yeager has further taught placing results of the addition in the renamed destination register. (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

g) preventing the propagation of a carryover of the addition results from low-order bit positions of the renamed destination register to high-order bit positions of the renamed destination register. See Blomgren, Fig.2, and note that in the case of the ADD BH,AL->AL instruction, adder 164 will add two 8-bit numbers and produce an 8-bit result. Even if both numbers were 11111111, which when added would normally produce a carry, adder 164 does not produce or propagate a carry. See column 11, lines 25-29.

19. Referring to claims 29 and 32, Blomgren in view of Yeager has taught a method as described in claim 28. Blomgren has further taught that screening the first and second renamed source registers comprises: modifying contents of one of the renamed source register by setting low order bits of the one of the renamed source registers to zero; and modifying the contents of the other renamed source register by setting high order bits of the other source register to zero (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the instruction ADD BL,AH->AH the lower portion of B is added to the middle portion of A, which results in the counterparts being zeroed).

20. Referring to claims 30 and 33, Blomgren in view of Yeager has taught a method as described in claim 29. Blomgren has further taught that merging the operation results comprises: adding the modified contents of the one of the renamed source registers with the modified contents of the other renamed source register; and placing results of the addition into the renamed destination register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

23. Claims 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren in view of Yeager, as applied above, and further in view of Shippy, U.S. Patent Number 6,003,125 (as applied in the previous Office Action).

25. Referring to claims 38-42, Blomgren in view of Yeager has taught a method as described in claim 11. Blomgren in view of Yeager has not explicitly taught that propagating a carryover result is accomplished by Anding the carryover result with a carry enable and said preventing propagation of a carryover result comprises removing said carry enable to prevent propagation of the carryover result. Shippy has taught wherein propagating a carryover result is accomplished by Anding the carryover result with a carry enable and said preventing propagation of a carryover result comprises removing said carry enable to prevent propagation of the carryover result (Shippy abstract, figure 3, column 2 line 50-column 3 line 7). Blomgren does show that carry bits must be taken from the lower adders to the higher adders when a full add takes place, and has also taught not using the carry bit when part of the source register is to be passed from the execution unit, unchanged (Blomgren, figure 2, column 11 lines 25-29). However, Blomgren does not go into detail how he prevents, or turns off and on, the carryover bit in the higher adders when it is not needed. One of ordinary skill in the art would have recognized, that Shippy provides the details of how to control the carryover bit between a high and low level adder, and thus would enable one of ordinary skill in the art at the time of the invention to build a design of Blomgren's system using the enable and gate to control the carryover between adders. It is inherent that Blomgren must control the carryover bit in some fashion, because sometimes the carry bit is used in a full add, and sometimes the carry bit is ignored when it is a partial add. Implementing a single and-gate, and using a signal coming from the control unit that is driven by

the unique opcode that is associated with each instruction can allow the system to control the carryover bit in the system of Blomgren. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an enable and-gate with an enable signal to control the carryover bit being used by the higher adder in the system of Blomgren, to allow one of ordinary skill in the art to make a detailed design, and be able to build a functioning system.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the

references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hennessy and Patterson, "Computer Architecture - A Quantitative Approach, 2nd Edition," 1996, pp. 232-233 and 251, has taught the basic concept of register renaming and how it is used to overcome WAW and WAR hazards.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 25, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER